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(54) Multiple sector erase flash EEPROM system

EEPROM-System mit aus mehreren Chips bestehender Blocklöschung

Système EEPROM avec effacement en bloc contenant des puces multiples

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Description

[0001] This invention relates generally to semiconductor electrically erasable programmable read only memories (EEProm), and specifically to a system of integrated circuit Flash EEPROM chips.

[0002] Computer systems typically use magnetic disk drives for mass storage of data. However, disk drives are disadvantageous in that they are bulky and in their requirement for high precision moving mechanical parts. Consequently they are not rugged and are prone to reliability problems, as well as consuming significant amounts of power. Solid state memory devices such as DRAM's and SRAM's do not suffer from these disadvantages. However, they are much more expensive, and require constant power to maintain their memory (volatile). Consequently, they are typically used as temporary storage.

[0003] EEPROM's and Flash EEPROM's are also solid state memory devices. Moreover, they are nonvolatile, and retain their memory even after power is shut down. However, conventional Flash EEPROM's have a limited lifetime in terms of the number of write (or program)/erase cycles they can endure. Typically the devices are rendered unreliable after 10^2 to 10^3 write/erase cycles. Traditionally, they are typically used in applications where semi-permanent storage of data or program is required but with a limited need for reprogramming.

[0004] It is the object of the present invention to provide a Flash EEPROM system and method thereof with improved erase operation.

[0005] This object is solved by the subject matter of the independent claims.

[0006] Preferred embodiments of the present invention are defined by the dependent claims.

[0007] These and additional aspects are accomplished by improvements in the architecture of a system of EEPROM chips, and the circuits and techniques therein.

[0008] According to one aspect of the present invention, an array of Flash EEPROM cells on a chip is organized into sectors such that all cells within each sector are erasable at once. A Flash EEPROM memory system comprises one or more Flash EEPROM chips under the control of a controller. The invention allows any combination of sectors among the chips to be selected and then erased simultaneously. This is faster and more efficient than prior art schemes where all the sectors must be erased every time or only one sector at a time can be erased. The invention further allows any combination of sectors selected for erase to be deselected and prevented from further erasing during the erase operation. This feature is important for stopping those sectors that are first to be erased correctly to the "erased" state from over erasing, thereby preventing unnecessary stress to the Flash EEPROM device. The invention also allows a global de-select of all sectors in the system so that no sectors are selected for erase. This global reset can

quickly put the system back to its initial state ready for selecting the next combination of sectors for erase. Another feature of the invention is that the selection is independent of the chip select signal which enables a particular chip for read or write operation. Therefore it is possible to perform an erase operation on some of the Flash EEPROM chips while read and write operations may be performed on other chips not involved in the erase operation.

[0009] Additional aspects, features, and advantages of the present invention will be understood from the following description of its preferred embodiments, which description should be taken in conjunction with the accompanying drawings.

Fig. 1A is a general microprocessor system including the Flash EEPROM memory system of the present invention;

Fig. 1B is schematic block diagram illustrating a system including a number of Flash EEPROM memory chips and a controller chip;

Fig. 2 is a schematic illustration of a system of Flash EEPROM chips, among which memory sectors are selected to be erased;

Fig. 3A is a block circuit diagram on a Flash EEPROM chips for implementing selective multiple sector erase according to the preferred embodiment;

Fig. 3B shows details of a typical register used to select a sector for erase as shown in Fig. 2A;

Fig. 4 is a flow diagram illustrating the erase sequence of selective multiple sector erase.

Description of the Preferred Embodiments

EEProm System

[0010] A computer system in which the various aspects of the present invention are incorporated is illustrated generally in Figure 1A. A typical computer system architecture includes a microprocessor 21 connected to a system bus 23, along with random access, main system memory 25, and at least one or more input-output devices 27, such as a keyboard, monitor, modem, and the like. Another main computer system component that is connected to a typical computer system bus 23 is a large amount of long-term, non-volatile memory 29. Typically, such a memory is a disk drive with a capacity of tens of megabytes of data storage. This data is retrieved into the system volatile memory 25 for use in current processing, and can be easily supplemented, changed or altered.

[0011] One aspect of the present invention is the substitution of a specific type of semiconductor memory system for the disk drive but without having to sacrifice non-volatility, ease of erasing and rewriting data into the memory, speed of access, low cost and reliability. This is accomplished by employing an array of electrically erasable programmable read only memories (EEP-

rom's) integrated circuit chips. This type of memory has additional advantages of requiring less power to operate, and of being lighter in weight than a hard disk drive magnetic media memory, thereby being especially suited for battery operated portable computers.

[0012] The bulk storage memory 29 is constructed of a memory controller 31, connected to the computer system bus 23, and an array 33 of EEPROM integrated circuit chips. Data and instructions are communicated from the controller 31 to the EEPROM array 33 primarily over a serial data line 35. Similarly, data and status signals are communicated from the EEPROM array 33 to the controller 31 over serial data lines 37. Other control and status circuits between the controller 31 and the EEPROM array 33 are not shown in Figure 1A.

[0013] Referring to Figure 1B, the controller 31 is preferably formed primarily on a single integrated circuit chip. It is connected to the system address and data bus 39, part of the system bus 33, as well as being connected to system control lines 41, which include interrupt, read, write and other usual computer system control lines.

[0014] The EEPROM array 33 includes a number of EEPROM integrated circuit chips 43, 45, 47, etc. Each includes a respective chip select and enable line 49, 51 and 53 from interface circuits 40. The interface circuits 40 also act to interface between the serial data lines 35, 37 and a circuit 55. Memory location addresses and data being written into or read from the EEPROM chips 43, 45, 47, etc. are communicated from a bus 55, through logic and register circuits 57 and thence by another bus 59 to each of the memory chips 43, 45, 47 etc.

[0015] The bulk storage memory 29 of Figures 1A and 1B can be implemented on a single printed circuit card for moderate memory sizes. The various lines of the system buses 39 and 41 of Figure 1B are terminated in connecting pins of such a card for connection with the rest of the computer system through a connector. Also connected to the card and its components are various standard power supply voltages (not shown).

[0016] For large amounts of memory, that which is conveniently provided by a single array 33 may not be enough. In such a case, additional EEPROM arrays can be connected to the serial data lines 35 and 37 of the controller chip 31, as indicated in Figure 1B. This is preferably all done on a single printed circuit card but if space is not sufficient to do this, then one or more EEPROM arrays may be implemented on a second printed circuit card that is physically mounted onto the first and connected to a common controller chip 31.

Erase of Memory Structures

[0017] In system designs that store data in files or blocks the data will need to be periodically updated with revised or new information. It may also be desirable to overwrite some no longer needed information, in order to accommodate additional information. In a Flash EEPROM

memory, the memory cells must first be erased before information is placed in them. That is, a write (or program) operation is always preceded by an erase operation.

[0018] In conventional Flash erase memory devices, the erase operation is done in one of several ways. For example, in some devices such as the Intel corporation's model 27F-256 CMOS Flash EEPROM, the entire chip is erased at one time. If not all the information in the chip is to be erased, the information must first be temporarily saved, and is usually written into another memory (typically RAM). The information is then restored into the nonvolatile Flash erase memory by programming back into the device. This is very slow and requires extra memory as holding space.

[0019] In other devices such as Seeq Technology incorporated's model 48512 Flash EEPROM chip, the memory is divided into blocks (or sectors) that are each separately erasable, but only one at a time. By selecting the desired sector and going through the erase sequence the designated area is erased. While, the need for temporary memory is reduced, erase in various areas of the memory still requires a time consuming sequential approach.

[0020] In the present invention, the Flash EEPROM memory is divided into sectors where all cells within each sector are erasable together. Each sector can be addressed separately and selected for erase. One important feature is the ability to select any combination of sectors for erase together. This will allow for a much faster system erase than by doing each one independently as in prior art.

[0021] Figure 2 illustrates schematically selected multiple sectors for erase. A Flash EEPROM system includes one or more Flash EEPROM chips such as 201, 203, 205. They are in communication with a controller 31 through lines 209. Typically, the controller 31 is itself in communication with a microprocessor system (not shown). The memory in each Flash EEPROM chip is partitioned into sectors where all memory cells within a sector are erasable together. For example, each sector may have 512 bytes (i.e. 512x8 cells) available to the user, and a chip may have 1024 sectors. Each sector is individually addressable, and may be selected, such as sectors 211, 213, 215, 217 in a multiple sector erase. As illustrated in figure 2, the selected sectors may be confined to one EEPROM chip or be distributed among several chips in a system. The sectors that were selected will all be erased together. This capability will allow the memory and system of the present invention to operate much faster than the prior art architectures.

[0022] Figure 3A illustrates a block diagram circuit 220 on a Flash EEPROM chip (such as the chip 201 of figure 2) with which one or more sectors such as 211, 213 are selected (or deselected) for erase. Essentially, each sector such as 211, 213 is selected or tagged by setting the state of an erase enable register such as 221, 223 associated with the respective sectors. The selec-

tion and subsequent erase operations are performed under the control of the controller 31 (see figure 2). The circuit 220 is in communication with the controller 31 through lines 209. Command information from the controller is captured in the circuit 220 by a command register 225 through a serial interface 227. It is then decoded by a command decoder 229 which outputs various control signals. Similarly, address information is captured by an address register 231 and is decoded by an address decoder 233.

[0023] For example, in order to select the sector 211 for erase, the controller sends the address of the sector 211 to the circuit 220. The address is decoded in line 235 and is used in combination with a set erase enable signal in bus 237 to set an output 239 of the register 221 to HIGH. This enables the sector 211 in a subsequent erase operation. Similarly, if the sector 213 is also desired to be erased, its associated register 223 may be set HIGH.

[0024] Figure 3B shows the structure of the register such as 221, 223 in more detail. The erase enable register 221 is a SET/RESET latch. Its set input 241 is obtained from the set erase enable signal in bus 237 gated by the address decode in line 235. Similarly, the reset input 243 is obtained from the clear erase enable signal in bus 237 gated by the address decode in line 235. In this way, when the set erase enable signal or the clear erase enable signal is issued to all the sectors, the signal is effective only on the sector that is being addressed.

[0025] After all sectors intended for erase have been selected, the controller then issues to the circuit 220, as well as all other chips in the system a global erase command in line 251 along with the high voltage for erasing in line 209. The device will then erase all the sectors that have been selected (i.e. the sectors 211 and 213) at one time. In addition to erasing the desired sectors within a chip, the architecture of the present system permits selection of sectors across various chips for simultaneous erase.

[0026] Figures 4(1)-4(11) illustrate the algorithm used in conjunction with the circuit 220 of figure 3A. In figure 4(1), the controller will shift the address into the circuit 220 which is decoded in the line to the erase enable register associated with the sector that is to be erased. In figure 4(2), the controller shifts in a command that is decoded to a set erase enable command which is used to latch the address decode signal onto the erase enable register for the addressed sector. This tags the sector for subsequent erase. In figure 4(3), if more sectors are to be tagged, the operations described relative to figures 4(1)-4(2) are repeated until all sectors intended for erase have been tagged. After all sectors intended for erase have been tagged, the controller initiates an erase cycle as illustrated in figure 4(4).

[0027] Optimized erase implementations have been disclosed in U.S. patents 5,095,344, 5,172,338 and 5,163,021. The disclosures of these patents are hereby incorporated by reference. The Flash EEPROM cells are

erased by applying a pulse of erasing voltage followed by a read to verify if the cells are erased to the "erased" state. If not, further pulsing and verifying are repeated until the cells are verified to be erased. By erasing in this controlled manner, the cells are not subject to over-erase which tends to age the EEPROM device prematurely as well as make the cells harder to program.

[0028] As the group of selected sectors is going through the erase cycle, some sectors will reach the "erase" state earlier than others. Another important feature of the present invention is the ability to remove those sectors that have been verified to be erased from the group of selected sectors, thereby preventing them from over-erasing.

[0029] Returning to figure 4(4), after all sectors intended for erase have been tagged, the controller initiates an erase cycle to erase the group of tagged sectors.

In figure 4(5), the controller shifts in a global command called Enable Erase into each Flash EEPROM chip that is to perform an erase. This is followed in figure 4(5) by the controller raising of the erase voltage line (V_{er}) to a specified value for a specified duration. The controller will lower this voltage at the end of the erase duration time. In figure 4(6), the controller will then do a read verify sequence on the sectors selected for erase. In figure 4(7), if none of the sectors are verified, the sequences illustrated in figures 4(5)-4(7) are repeated. In figures 4(8) and 3(9), if one or more sectors are verified to be erased, they are taken out of the sequence. Referring also to figure 3A, this is achieved by having the controller address each of the verified sectors and clear the associated erase enable registers back to a LOW with a clear enable command in bus 237. The sequences illustrated in figures 4(5)-4(10) are repeated until all the sectors in the group are verified to be erased in figure 4(11). At the completion of the erase cycle, the controller will shift in a No Operation (NOP) command and the global Enable Erase command will be withdrawn as a protection against a false erasure.

[0030] The ability to select which sectors to erase and which ones not to, as well as which ones to stop erasing is advantageous. It will allow sectors that have erased before the slower erased sectors to be removed from the erase sequence so no further stress on the device will occur. This will increase the reliability of the system. Additional advantage is that if a sector is bad or is not used for some reason, that sector can be skipped over with no erase occurring within that sector. For example, if a sector is defective and have shorts in it, it may consume much power. A significant system advantage is gained by the present invention which allows it to be skipped on erase cycles so that it may greatly reduce the power required to erase the chip.

[0031] Another consideration in having the ability to pick the sectors to be erased within a device is the power savings to the system. The flexibility in erase configuration of the present invention enables the adaptation of the erase needs to the power capability of the system.

This can be done by configuring the systems to be erased differently by software on a fixed basis between different systems. It also will allow the controller to adaptively change the amount of erasing being done by monitoring the voltage level in a system, such as a laptop computer.

[0032] An additional performance capability of the system in the present invention is the ability to issue a reset command to a Flash EEPROM chip which will clear all erase enable latches and will prevent any further erase cycles from occurring. This is illustrated in figures 3A and 3B by the reset signal in the line 261. By doing this in a global way to all the chips, less time will be taken to reset all the erase enable registers.

[0033] An additional performance capability is to have the ability to do erase operations without regard to chip select. Once an erase is started in some of the memory chips, the controller in the system can access other memory chips and do read and write operations on them. In addition, the device(s) doing the erase can be selected and have an address loaded for the next command following the erase.

[0034] The various aspects of the present invention that have been described co-operate in a system of Flash EEPROM memory array to make the Flash EEPROM memory a viable alternative to conventional non-volatile mass storage devices.

[0035] While the embodiments of the various aspects of the present invention that have been described are the preferred implementation, those skilled in the art will understand that variations thereof may also be possible. Therefore, the invention is entitled to protection within the full scope of the appended claims.

Claims

1. A method of operating a memory system having an array of EEPROM cells divided into multiple sectors that individually contain a plurality of said cells sufficient to store multiple bytes of data, and wherein all cells of a sector are erasable together, comprising:

- (a) selecting a plurality of said multiple sectors to be erased,
- (b) erasing the EEPROM cells of the selected sectors together while the non-selected sectors are not erased,
- (c) thereafter verifying whether individual ones of the selected sectors have become erased, and
- (d) deselecting those sectors which are verified to have become erased.

2. The method of claim 1, further comprising a step (e) of repeating operations (b) through (d) until all of the initially selected sectors have been deselected.

3. The method of claim 2, further comprising a step (f) of writing data in at least some of the erased sectors.

4. The method of any of claims 1 to 3, wherein step (b) comprises erasing the selected sectors in parallel.

5. The method of claim 4, which additionally comprises adaptively changing the number of sectors that are erased in parallel according to a power capability of the system.

6. The method of any of claims 1 to 5, which additionally comprises maintaining an identification of those of said multiple sectors that are defective, and avoiding subjecting such identified sectors to the erasing step.

7. The method of any of claims 1 to 6, wherein step (a) comprises selecting a plurality of but less than all of said multiple sectors to be erased.

8. The method of any of claims 1 to 7, wherein step (a) comprises setting a tag bit for individual ones of the sectors to be selected, and wherein step (d) comprises clearing the tag bits for the sectors to be deselected.

9. The method of any of claims 1 to 8, wherein step (b) comprises erasing the selected sectors by subjecting them to erase voltages.

10. A flash EEPROM system, comprising:

an array of EEPROM cells divided into multiple sectors that individually contain a plurality of said cells for individually storing multiple bytes of data, the cells of the individual sectors being erasable together,
a select circuit for selecting a plurality of said multiple sectors,
an erase circuit for erasing together all the selected sectors without erasing the sectors that are not selected,
verifying means for verifying whether individual ones of the selected sectors have become erased, and

wherein the select circuit further comprises means for deselecting those sectors which are verified to have become erased.

11. The system of claim 10, wherein the erase circuit is adapted for erasing the selected sectors in parallel.

12. The system of claim 11, further comprising controller means for adaptively changing the number of

sectors that are erased in parallel according to a power capability of the memory system.

13. The system of any of claims 10 to 12, further comprises means for maintaining an identification of those of said multiple sectors that are defective, and means for avoiding subjecting such identified sectors to the erasing step.
14. The system of any of claims 10 to 13, wherein the select circuit is further adapted for selecting any combination of the selected plurality of but less than all of said multiple sectors.
15. The system of any of claims 10 to 14, wherein the select circuit comprises a plurality of registers that individually contain a tag indicating whether an associated sector is selected or not.
16. The system of claim 15, wherein the select circuit is further adapted for setting the tag for individual ones of the sectors selected for erasure and for clearing the tag bits for the sectors which are verified to be erased.
17. The system of any of claims 10 to 16, wherein the EEPROM array comprises multiple EEPROM chips.
18. The system of claim 17, wherein the selected sectors are confined to one of said multiple EEPROM chips.
19. The system of claim 17, wherein the selected sectors are distributed among several of said multiple EEPROM chips.
20. The system of any of claims 10 to 19, further comprising a system controller for controlling the system and a system address bus for connecting the system with the system controller.

Patentansprüche

1. Verfahren zum Betreiben eines Speichersystems, welches eine in mehrere Sektoren unterteilte Matrix aus EEPROM-Zellen aufweist, die individuell eine zum Speichern von mehreren Datenbytes ausreichende Vielzahl besagter Zellen beinhalten, und wobei alle Zellen eines Sektors gemeinsam löscherbar sind, umfassend:
(a) Auswählen einer Vielzahl von besagten mehreren Sektoren zum Löschen,
(b) gemeinsames Löschen der EEPROM-Zellen der ausgewählten Sektoren, wobei die nicht ausgewählten Sektoren nicht gelöscht werden,

(c) anschließendes Verifizieren, ob einzelne der ausgewählten Sektoren gelöscht worden sind, und

(d) Entfernen derjenigen Sektoren aus der Auswahl, die als gelöscht geworden zu sein verifiziert sind.

2. Verfahren nach Anspruch 1, weiter umfassend einen Schritt (e) des Wiederholens der Verfahrensschritte (b) bis (d) so lange, bis alle der ursprünglich ausgewählten Sektoren von der Auswahl entfernt worden sind.
3. Verfahren nach Anspruch 2, weiter umfassend einen Schritt (f) des Schreibens von Daten in zumindest einige der gelöschten Sektoren.
4. Verfahren nach einem der Ansprüche 1 bis 3, wobei der Schritt (b) ein paralleles Löschen der ausgewählten Sektoren umfasst.
5. Verfahren nach Anspruch 4, welches zusätzlich ein adaptives Ändern der Anzahl der parallel zu löschenden Sektoren gemäß einer Leistungsfähigkeit des Systems umfasst.
6. Verfahren nach einem der Ansprüche 1 bis 5, welches zusätzlich ein Beibehalten einer Identifikation derjenigen der besagten mehreren Sektoren umfasst, welche fehlerhaft sind, und ein Vermeiden, dass solche identifizierte Sektoren dem Löschschritt ausgesetzt werden, umfasst.
7. Verfahren nach einem der Ansprüche 1 bis 6, wobei der Schritt (a) ein Auswählen einer Vielzahl von den doch weniger als alle der besagten mehreren Sektoren zur Löschung umfasst.
8. Verfahren nach einem der Ansprüche 1 bis 7, wobei der Schritt (a) ein Setzen eines Markierungsbits für einzelne dieser Sektoren umfasst, um ausgewählt zu werden, und worin Schritt (d) ein Aufheben der Markierungsbits für die Sektoren umfasst, die von der Auswahl entfernt werden.
9. Verfahren nach einem der Ansprüche 1 bis 8, wobei der Schritt (b) ein Löschen der ausgewählten Sektoren umfasst, indem diese Löschespannungen ausgesetzt werden.
10. Flash-EEPROM-System, umfassend:

eine Matrix aus EEPROM-Zellen, welche in mehrere Sektoren, die individuell eine Vielzahl dieser Zellen zum individuellen Speichern mehrerer Datenbytes beinhalten, unterteilt ist, wobei die Zellen der individuellen Sektoren zusammen löscherbar sind,

eine Auswählschaltung zum Auswählen einer Vielzahl besagter mehrerer Sektoren,

eine Löschschtaltung zum gemeinsamen Löschen aller ausgewählter Sektoren ohne Löschen der nicht ausgewählten Sektoren,

Verifikationsmittel zum Verifizieren, ob einzelne der ausgewählten Sektoren gelöscht wurden, und

wobei die Auswählschaltung weiterhin Mittel zum Entfernen solcher Sektoren aus der Auswahl umfasst, welche als gelöscht worden zu sein verifiziert sind.

11. System nach Anspruch 10, wobei die Löschschtaltung zum parallelen Löschen der ausgewählten Sektoren angepasst ist.
12. System nach Anspruch 11, weiter umfassend Steuermittel zum adaptiven Ändern der Anzahl von Sektoren, die parallel gelöscht werden, gemäß einer Leistungsfähigkeit des Speichersystems.
13. System nach einem der Ansprüche 10 bis 12, weiter umfassend Mittel zum Beibehalten einer Identifikation von solchen von den besagten mehreren Sektoren, die fehlerhaft sind, und Mittel zum Vermeiden, dass diese identifizierte Sektoren dem Löschschnitt ausgesetzt werden.
14. System nach einem der Ansprüche 10 bis 13, wobei die Auswählschaltung weiter angepasst ist, jede Kombination der ausgewählten Vielzahl von den doch weniger als alle der besagten mehreren Sektoren auszuwählen.
15. System nach einem der Ansprüche 10 bis 14, wobei die Auswählschaltung eine Vielzahl von Registern umfasst, die individuell ein Markierungsbit zum Anzeigen, ob ein zugehöriger Sektor ausgewählt ist oder nicht, beinhalten.
16. System nach Anspruch 15, wobei der Auswählschaltkreis weiter angepasst ist, die Markierung für einzelne der zum Löschen ausgewählten Sektoren zu setzen und die Markierungsbits für die Sektoren zurückzusetzen, welche als gelöscht zu sein verifiziert sind.
17. System nach einem der Ansprüche 10 bis 16, wobei die EEPROM-Matrix mehrere EEPROM-Chips umfasst.
18. System nach Anspruch 17, wobei die ausgewählten Sektoren auf einen der besagten mehreren EEPROM-Chips beschränkt sind.

19. System nach Anspruch 17, wobei die ausgewählten Sektoren auf verschiedene der besagten mehreren EEPROM-Chips verteilt sind.

20. System nach einem der Ansprüche 10 bis 19, weiter umfassend eine Systemsteuerung zum Steuern des Systems und einen Systemadressbus zum Verbinden des Systems mit der Systemsteuerung.

Revendications

1. Procédé pour faire fonctionner un système de mémoire ayant une matrice de cellules EEPROM divisée en multiples secteurs qui contiennent individuellement une pluralité dedites cellules, suffisante pour stocker de multiples octets de données, et dans lequel toutes les cellules d'un secteur sont effaçables ensemble, comprenant les étapes suivantes :
 - (a) sélectionner une pluralité dedites multiples secteurs à effacer,
 - (b) effacer les cellules EEPROM des secteurs sélectionnés ensemble tandis que les secteurs non sélectionnés ne sont pas effacés,
 - (c) vérifier ensuite si des secteurs individuels parmi les secteurs sélectionnés ont été effacés, et
 - (d) désélectionner les secteurs qui sont vérifiés comme étant devenus effacés.
2. Procédé de la revendication 1, comprenant en outre une étape (e) consistant à répéter les étapes (b) à (d) jusqu'à ce que tous les secteurs initialement sélectionnés aient été désélectionnés.
3. Procédé de la revendication 2, comprenant en outre une étape (f) consistant à écrire des données dans au moins certains des secteurs effacés.
4. Procédé selon l'une quelconque des revendications 1 à 3, dans lequel l'étape (b) comprend l'effacement des secteurs sélectionnés en parallèle.
5. Procédé de la revendication 4, qui comprend en outre un changement adaptatif du nombre des secteurs qui sont effacés en parallèle selon une capacité de puissance du système.
6. Procédé selon l'une quelconque des revendications 1 à 5, comprenant en outre le maintien d'une identification de ceux desdits multiples secteurs qui sont défectueux, et le fait d'éviter de soumettre de tels secteurs identifiés à l'étape d'effacement.
7. Procédé selon l'une quelconque des revendications 1 à 6, dans lequel l'étape (a) comprend la sélection

d'une pluralité de secteurs, mais moins que la totalité desdits multiples secteurs à effacer.

8. Procédé selon l'une quelconque des revendications 1 à 7, dans lequel l'étape (a) comprend la définition d'un bit d'étiquette pour des secteurs individuels parmi les secteurs à sélectionner, et dans lequel l'étape (d) comprend l'effacement des bits d'étiquette pour les secteurs à désélectionner.

9. Procédé selon l'une quelconque des revendications 1 à 8, dans lequel l'étape (b) comprend l'effacement des secteurs sélectionnés en les soumettant à des tensions d'effacement.

10. Système EEPROM flash comprenant :

une matrice de cellules EEPROM divisée en multiples secteurs qui contiennent individuellement une pluralité desdites cellules pour stocker individuellement de multiples octets de données, les cellules des secteurs individuels étant effaçables ensemble, un circuit de sélection pour sélectionner une pluralité desdits multiples secteurs, un circuit d'effacement pour effacer ensemble tous les secteurs sélectionnés sans effacer les secteurs qui ne sont pas sélectionnés, des moyens de vérification pour vérifier si des secteurs individuels parmi les secteurs sélectionnés sont devenus effacés, et

dans lequel le circuit de sélection comprend en outre des moyens pour désélectionner ces secteurs qui sont vérifiés comme étant devenus effacés.

11. Système de la revendication 10, dans lequel le circuit d'effacement est adapté pour effacer les secteurs sélectionnés en parallèle.

12. Système de la revendication 11, comprenant en outre des moyens de contrôleur pour modifier de manière adaptative le nombre des secteurs qui sont effacés en parallèle selon une capacité de puissance du système de mémoire.

13. Système selon l'une quelconque des revendications 10 à 12, comprenant en outre des moyens pour maintenir une identification de ceux desdits multiples secteurs qui sont défectueux, et des moyens pour éviter de soumettre de tels secteurs identifiés à l'étape d'effacement.

14. Système selon l'une quelconque des revendications 10 à 13, dans lequel le circuit de sélection est en outre adapté pour sélectionner toute combinaison de la pluralité sélectionnée de multiples sec-

teurs, mais moins que la totalité desdits multiples secteurs.

15. Système selon l'une quelconque des revendications 10 à 14, dans lequel le circuit de sélection comprend une pluralité de registres qui contiennent individuellement une étiquette indiquant si un secteur associé est sélectionné ou non.

16. Système de la revendication 15, dans lequel le circuit de sélection est en outre adapté pour définir l'étiquette pour des secteurs individuels parmi les secteurs sélectionnés pour l'effacement et pour supprimer les bits d'étiquette pour les secteurs dont on a vérifié qu'ils ont été effacés.

17. Système selon l'une quelconque des revendications 10 à 16, dans lequel la matrice d'EEPROM comprend de multiples circuits intégrés EEPROM.

18. Système de la revendication 17, dans lequel les secteurs sélectionnés sont confinés à l'un desdits multiples circuits intégrés EEPROM.

19. Système de la revendication 17, dans lequel les secteurs sélectionnés sont distribués entre plusieurs desdits multiples circuits intégrés EEPROM.

20. Système selon l'une quelconque des revendications 10 à 19, comprenant en outre un contrôleur de système pour contrôler le système et un bus d'adresses de système pour connecter le système au contrôleur de système.

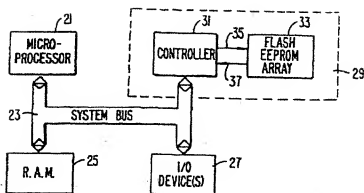


FIG. 1A.

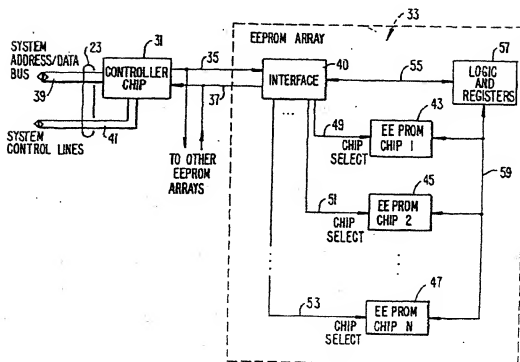
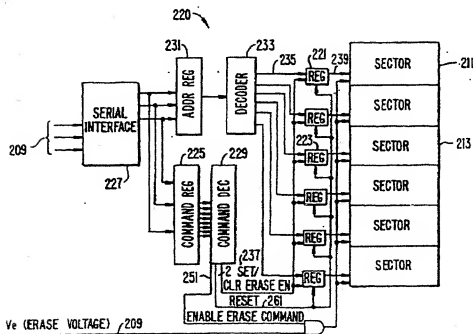
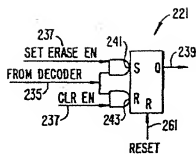
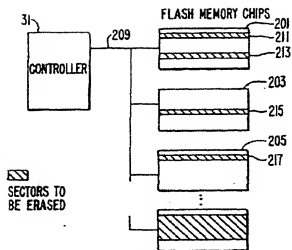


FIG. 1B.



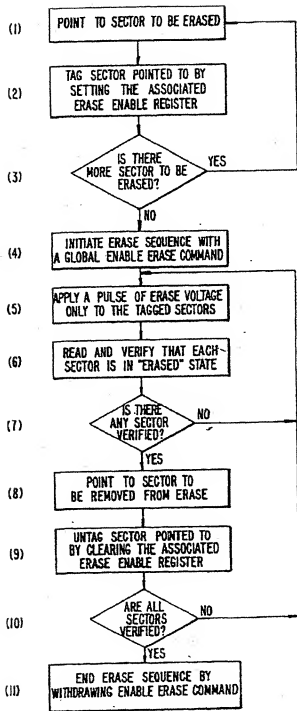


FIG. 4.